A NOVEL 1-BIT HYBRID FULL ADDER IN 90NM AND 180NM TECHNOLOGIES

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ABSTRACT
It has been stated that transmission gate logic and complementary metal-oxide-semiconductor (CMOS) can be used to create a 1-bit full adder. Support for 32 bits was later added to the initial design, which was created for 1 bit. The circuit was constructed using Cadence Virtuoso tools in both 90 and 180 nm technologies. Measurements of power, delay, and layout area were made and compared to comparable existing systems, such as complementary pass-transistor logic, hybrid pass-logic with static CMOS output drive full adders, gearbox gate adders, and gearbox function adders. For a 1.8-V supply at 180-nm technology, the purposeful combination of powerful transmission gates and very weak CMOS inverters produced an incredibly low average power consumption (4.232 W) and a comparatively low latency (226 ps). At 1.2. For 90 nm technology and V supply voltage, the equivalent values were 98 ps and 1.1965 W. It was found that the new method performs noticeably better in terms of speed and power than the current full adder designs.

I. INTRODUCTION

For 90 nm technology and V supply voltage, the equivalent values were 98 ps and 1.1965 W. It was found that the new method performs noticeably better in terms of speed and power than the current full adder designs..

1.1 OVERVIEW

A single transistor was the main component ofeach semiconductor. The number of transistors increased in later developments, enabling the addition of a greater range of specialized features and systems. One or more logical doors could be produced on a single device in the past because integrated circuits were composed of a small number of devices—possibly as few as ten diodes, transistors, resistors, and capacitors. The growth of large scale incorporation (LSI), or frameworks with at least a thousand rational entryways, was aided by procedural advancements that resulted in devices with numerous rational entryways, presently reflectively referred to as "little scale joining" (SSI). Chips today have millions of gates and many individual transistors, demonstrating how far modern technology has advanced from this model. There was Previously, there was an attempt to categorize and refine the several types of large-scale integration that are not VLSI. "Ultra-substantial-scale Integration" (ULSI) was one of the terms we utilized. However, such nitpicking has become irrelevant due to the wide variety of ports and transistors found in everyday electronics. Terms that suggest integration levels higher than VLSI are no longer used as frequently. In fact, given the widespread perception that all chips are VLSI or better, even VLSI is now fairly interesting. Previously, there was an attempt to categorize and refine the several types of large-scale integration that are not VLSI. "Ultra-substantial-scale Integration" (ULSI) was one of the terms we utilized. However, such nitpicking has become irrelevant due to the wide variety of ports and transistors found in everyday electronics. The using of phrases that indicate The use of integration levels higher than VLSI has mostly decreased. In fact, given the widespread perception that all chips are VLSI or better, even VLSI is now fairly interesting.

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1.2 MOTIVATION

The addition operation is essential to all digital systems, including control systems and digital signal processing systems. The quality of a digital system's on-board adders has a significant impact on its dependability and efficiency. The majority of computer systems require adders because subtractions, multiplications, and divisions are also done digitally. By employing adders more skillfully, we can increase the system's efficiency. Our goal to advance the state of the art for upcoming generations drives us as ambitious engineers. To find out where we can increase the system's speed, power, and footprin, we are investigating adders.

1.3 WHAT IS VLSI?

The acronym for "Very Large Scale Integration" is VLSI. This field of study focuses on packing an increasing number of logic devices into a decreasing amount of space.The concentration of several transistors on a single silicon chip is known as Very Large Scale Integration, or VLSI. Electronic circuits that are extremely complex and small can be designed and manufactured using modified semiconductor material. Although integrated circuits (ICs) are employed in almost all electrical logic devices, each transistor on an IC is only a few millimeters in size.

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1.3.1 HISTORY OF SCALE INTEGRATION

Jack Kilby developed the first integrated circuit (JK-FF) at TI in the late 1950s. The early 1960s In the late 1960s, tens of transistors on a single chip were used for small-scale integration (SSI) and medium-scale integration (MSI). In the 1980s, there were 10,000 transistors on a chip; in the 1990s, there were 100,000; in the 2010s, there were one million; and for one million transistors on a chip, ultra LSI was occasionally utilized. Integration Scaled Down (from 0 to 102) (Pages 102–103) SSI Medium-Scale Integration (MSI). Integration on a Large Scale (LSI) (Page(s):(103–105) VLSI, or "Very Large Scale Integration" (pp. 105–107). Ultra Large-Scale Integration (>=107), or ULSI, is precisely that.

1.3.2 ADVANTAGES OF ICS OVER DISCRETE COMPONENTS

While our focus will be on ICs, it is important to note that the attributes of ICs (what can and cannot be efficiently put in an IC) heavily influence the design of the overall system. There are many essential ways in which integrated circuits enhance system features. There are three main benefits of ICs compared to discrete component digital circuits:

- Dimensions: Transistors and wires in integrated circuits are often measured in micrometres rather than the millimetres or centimetres used for discrete components. Since smaller components have less parasitic resistances, capacitances, and inductances, they are faster and use less power than their larger counterparts.
- Rapidity: Changing a signal from logic 0 to logic 1 within a semiconductor is substantially faster than doing it between chips. Inter-chip communication can be hundreds of times slower than intra-chip communication, yet intra-chip communication can occur on a printed circuit board. Smaller components and connections mean less signal slowing parasitic capacitance, which is why on-chip circuitry can operate at such fast speeds.
- In-chip logic processes also require significantly less power. Again, smaller circuits on the chip are mostly responsible for the reduced power consumption; their lower power requirements are a result of smaller parasitic capacitances and resistances.

1.3.3 VLSI AND SYSTEMS

These characteristics make integrated circuits more advantageous for the entire system: • Less clunky in appearance. Think about the advantages of portable cell phones and other little electronics. lower energy requirements. Power consumption significantly decreases when multiple common components are consolidated onto a single chip. Because of the reduction in power consumption, a simpler cabinet with less shielding for electromagnetic shielding may be possible, a smaller and less costly power supply can be used, and less power consumption equates to less heat, perhaps eliminating the need for a fan. • A reduced cost. Reducing the complexity of a system by removing extraneous components, supplies, cabinets, etc., can reduce its cost. Custom integrated circuits (ICs) can cost more than the standard ones, but By replacing traditional components, integration can have a cascading effect that lowers the whole cost of the system. Understanding why IC technology has such a profound impact on the design of digital systems requires knowledge of both the economics of ICs and digital systems as well as the technology of IC fabrication.

APPLICATIONS

- The electronic parts of automobiles.
- Digital electronics are used to operate VCRs.
- The Automated Teller Machine, or ATM • Computers, both at home and at work
- Digital medical records, etc..

1.3.4 APPLICATIONS OF VLSI

We rely on electronic devices for almost everything these days. Electronic systems, which are usually smaller, more flexible, and simpler to maintain, have occasionally taken the place of mechanisms that formerly operated mechanically, hydraulically, or in some other manner. However, electronic systems have occasionally led to whole new applications. Electronic systems serve a variety of purposes, some of which are more apparent than others. The electrical systems of the car regulate the music and display features, as well as the fuel injection, suspension, and anti-lock braking (ABS) systems. Portable media devices (MP3 players) and DVD players require surprisingly little power to perform complicated algorithms. • Digital electronics in consumer gadgets enable real-time video compression and decompression at high resolution data rates. • In spite of their specialized For this reason, even inexpensive Web browsing terminals need sophisticated circuitry. Today's desktop and laptop computers can be used for video games, financial analysis, and word processing. Both

general-purpose hardware, like a central processing unit (CPU), and specialized hardware, like hardware meant to speed up disk access or display, are found in computers. • Medical electronic systems use sophisticated processing algorithms to monitor internal operations and send out alarms. The availability of these intricate systems doesn't overwhelm clients; rather, it creates a need for even more intricate systems. Because of the growing complexity of their intended uses, integrated circuits and electronic systems are getting harder to design and produce. We create a growing range of general-purpose computers rather than just a few as systems get more complicated of special-purpose systems, which is arguably this group of systems' most impressive feature. Our accomplishments demonstrate our growing proficiency in integrated circuit design and manufacturing, but our clients' ever-increasing demands keep pushing us to the limit of our ability.

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II. LITERATURE SURVEY

Energy-efficient Smartphones, PDAs, laptops, and other battery-operated mobile devices have increased demand for VLSI and ultra large-scale integration (ULSI) designs. The complete adder has been a major focus of research for many years since it is one of the most crucial building blocks of all these circuit applications [1, 2]. Numerous logic techniques were used to study the implementation of 1-bit complete adder cells [3]–[11], each with unique advantages and disadvantages. Static styles and dynamic styles are the two broad categories into which the described designs can be divided. Because they are more stable, utilize less power, and occupy more space on the chip, static full adders are favored over their dynamic counterparts. There is a compromise in the way the different logic approaches perform. The most significant logic design types in the conventional realm are transmission gate full adder (TGA) [7], [8], static complementary metal-oxide-semiconductor (CMOS) [3], complementary pass-transistor logic (CPL) [5], [6], and dynamic CMOS logic [4]. The different adder designs that blend multiple logic types are referred to as hybrid-logic designs [9].These designs exploit the advantages of several logic approaches, which improves the performance of the complete adder. Although they require buffers and have a high input capacitance, standard complementary (CMOS) style-based adders (which have 28 transistors) are resistant to transistor sizing and voltage scaling [3]. One clever design of a complimentary type that consumes almost the same amount is the mirror adder [4] of power and transistors as the adder [3], but compared to a standard CMOS complete adder, it has a shorter maximum carry propagation path/delay inside the adder.In contrast, CPL efficiently restores voltage fluctuations by utilizing 32 transistors [5, 6]. However, when power usage is low, CPL is not a viable choice. Large transistor counts, static inverters, and input overloading from the high switching activity of intermediary nodes (increased switching power) are some of the problems that limit the approach. TGA effectively tackles the main issue of CPL, namely the voltage deterioration, with only 20 transistors required for full adder implementation [7], [8]. However, additional problems with CPL, such its slow speed and excessive power consumption, are concerning researchers.Scientists later focused on the hybrid logic..

III. EXISTING SYSTEM

3.1 ADDERS

You can manage anything if you know how to count to five. The addition operation is essential to all digital systems, including control systems and digital signal processing systems. The quality of a digital system's on-board adders has a significant impact on its dependability and efficiency. Adders are also a crucial component of digital systems due to their extensive use in other basic digital operations including division, multiplication, and subtraction. The time it takes for a circuit composed of such blocks to perform a binary operation would therefore be significantly reduced by speeding up the digital adder. The efficiency of a digital circuit block is assessed by calculating its processing speed, physical dimensions, and power consumption..

3.1.1 Basic Adder Unit

The most basic type of arithmetic is the addition of two binary values, or bits. A half adder is a combinational circuit that employs the following technique to add two bits. Three bits are processed simultaneously by a full adder, where the third bit is produced by the result of the first addition. One way to build a complete adder is to use two half adders. The whole adder serves as the foundational mathematical building block for all of the adders in this study.

3.1.2 Half Adder

A half adder can be used to add two binary digits, A and B, together. S, the sum of A and B, and Co, the matching carry, are produced. Although they aren't particularly useful by themselves, half adders make excellent building blocks for more intricate adding circuits (FA). A suggested implementation that substitutes an OR gate for an XOR gate, two AND gates, and two inverters is shown in Figure 2.1..

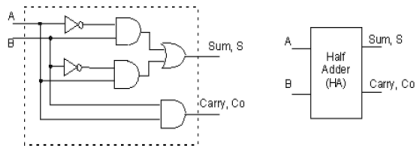

Figure 3.1: Block diagrams and logic for half-adding

Table 3.1 Half adder truth table

A	*B*	*S*	C_o
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Augend **A**
Addend **B**

Sum **C**

Boolean Equations:

$S = A \oplus B = A'B + AB'$

$Co = AB$

3.1.3 Full Adder

A complete adder is a combinational circuit that combines three bits (A, B, and C) with a carry in (Fig. 4.8.a) from the previous addition. The full adder produces the corresponding sum S and a carry out Co in the same manner as the half adder. As was previously indicated, two half adders can be connected in series to create a complete adder, as illustrated in Figure 2.2b. To obtain the final sum S, a second half adder receives the sum of A and B and combines it with the carry in C (from a previous addition operation). The ORed result of the carry outs from both half adders is Co, or the carry.

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Boolean Equations:

$$S = C \oplus (A \oplus B)$$

$$Co = AB + C(A \oplus B)$$

Table 3.2 Full Adder Truth Table

A	*B*	*C*	*S*	*Co*
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

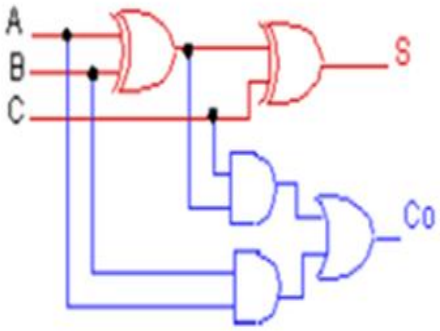

Figure 3.2a Full Adder

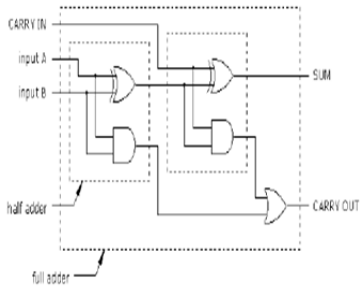

Figure 3.2b Combination full adder based on the use of two half adders

3.2 CONVENTIONAL CMOS FULL ADDER

The gate level implementation of a 28-transistor full adder and a standard CMOS full adder cell are shown in Figures 3.1 and 3.2. An entire adder cell with one bit has twenty-eight transistors. The CMOS design style is inefficient in terms of floor area for intricate gates with large fan-ins. To actualize a logic function, care must be taken when selecting a static logic style. Implementing pseudo NMOS is simple. It is commonly known

that pass transistors can be used to create specific logic circuits, including multiplexers and XOR-based circuits like adders. The traditional architecture of the conventional static CMOS full adder is based on a regular CMOS structure with normal pull-up and pull-down transistors that offer full swing output and good driving capabilities. Taking One method for building the whole adder circuit is to take the logic equation and translate it straight into a complementary CMOS circuit. Certain logical procedures can be used to decrease the number of transistors. As long as it doesn't slow down the carry production, which is the most important part, it is beneficial, for example, to share some logic between the sum and carry generating subcircuits. This is an illustration of a rearranged equation set.:

$$CARRY = A.B + B.Cin + A.Cin$$

$$SUM = A.B.Cin + CARRY(A + B + Cin)$$

Verifying if the new equations are comparable to the old ones is easy. This will require twenty-eight transistors. This circuit runs at a glacial rate in addition to taking up a lot of space..

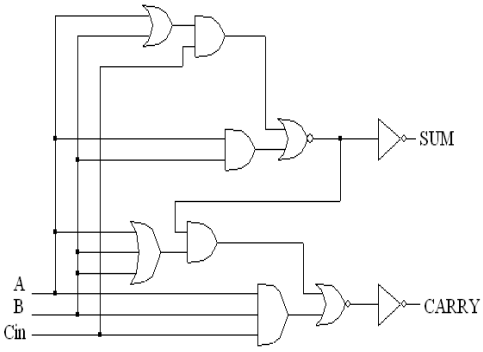

Fig 3.3: The entire adder is implemented using 28 transistors at the gate level.

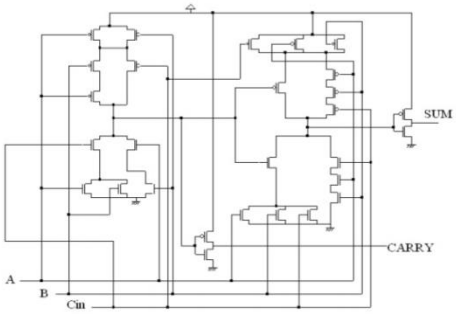

Fig 3.4: The entire adder is implemented in CMOS using 28 transistors.

3.3 TRANSMISSION GATE FULL ADDER

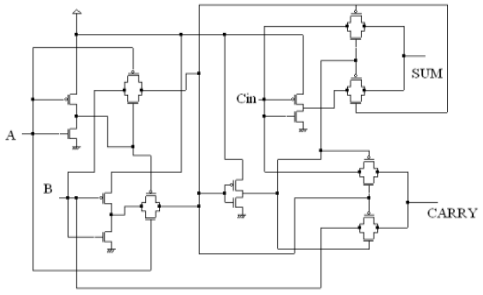

Fig 3.5: Full Adder Transmission Gate Architecture

Fig. 3.3 illustrates the design of a gearbox gate full adder, which has the advantage of generating sum and carry buffered outputs with the proper polarity but the disadvantage of using a lot of power.

Working principle In this circuit, two transmission gates that operate as an 8-T XOR come after two inverters. The circuit board for the 8-T XNOR comes next. The final sum is obtained by multiplexing Cin and Cin bar under the supervision of (a b) and (a b).The Cout can be calculated by multiplexing a and Cin, which are modulated by (a b**)..**

Advantage: It is the fastest adder ever recorded, as far as we are aware. Implementing the circuit is simpler than using a conventional adder..

Disadvantage: The power consumption of this circuit is greater than that of a 28T adder. But it uses the same amount of electricity and is more efficient..

3.4. 14T FULL ADDER CIRCUIT

The whole adder consists of 14 transistors, an inverter, two transmission gate designs, and a transmission gate-based multiplexer for sum and Cout signals. A 14T full adder was created by reducing the large transistor count of the traditional full adder using XOR and XNOR circuits based on pass transistor logic (see fig). Compared to earlier full adder trials, the development of the 14T full adder yielded improved results in terms of latency and power usage. The high-performance, low-power-dissipation multipliers were compatible with the 14T complete adder. The threshold power loss was not decreased by the adder, though. Additionally, the power consumption of the 14T adder is substantially higher than that of the 28T complete adder that is shown.

The 14-transistor adder, or 14T

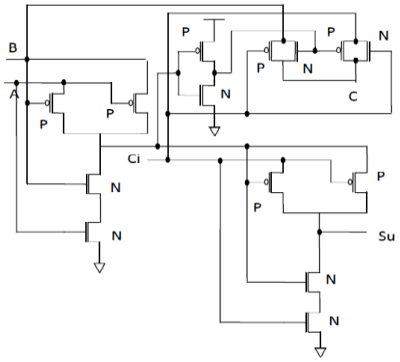

Fig. 3.6. The whole adder circuit for a 14-tuple

Fourteen transistors, two transmission gate designs, an inverter, and a transmission gate-based multiplexer for sum and Cout signals make up the entire adder. XOR and XNOR circuits based on pass transistor logic were used to reduce the huge transistor count of the conventional full adder, resulting in a 14T full adder (see fig). The creation of the 14T full adder produced better latency and power consumption outcomes than previous full adder testing. The 14T full adder worked well with the high-performance, low-power-dissipation multipliers. However, the adder did not reduce the threshold power loss. Furthermore, the 14T adder's power usage is significantly greater than that of the displayed 28T full adder.

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Working principle: This 4-transistor XOR circuit then switches to an XNOR. The total and cout are produced by combining XOR and XNOR. Either (a xor b) or (a b) can control the multiplexed cin and cinbar signals. Similarly, using (a b) as a guide, multiplexing a and cin will yield the cout. Benefit: To the best of our knowledge, it is the fastest adder ever recorded. The circuit is easier to implement than a traditional adder.

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Disadvantage: Compared to a 28T adder, this circuit uses more electricity. However, it is more efficient and consumes the same amount of electricity.

3.5. MIRROR ADDER

There are instances of symmetry between the nmos and pmos chains everywhere. Usually, carry generation circuits are made up of no more than two transistors coupled in series..

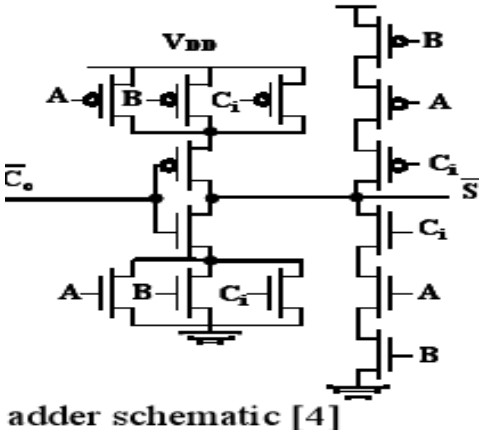

Fig. 3.7. Plan view of the Mirror Adder

The main goal of cell architecture is to minimize node capacitances. Cout shared diffusions can be used to reduce the capacitances at a stack's nodes. Near the final destination of the signal are transistors that are wired to cin. Only the carry stage transistors need to be adjusted for maximum velocity. During the summing stage, miniature transistors might be employed..

IV. PROPOSED SYSTEM

The three blocks in Fig. 1(a) represent the proposed full adder circuit. XNOR modules 1 and 2 generate the sum signal (SUM), whereas module 3 generates the carry signal (Cout). Each module for the adder circuit is designed with careful consideration for power, delay, and area. Below is a detailed examination of these components..

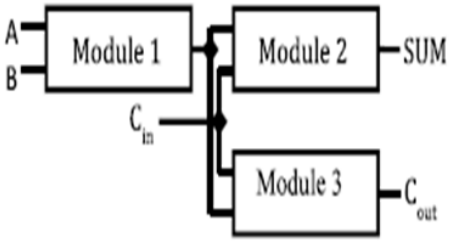

Fig. 4.1. The Proposed Full Adder, Shown as a Block Diagram

4.1 MODIFIED XNOR MODULE

In the suggested full adder circuit, the XNOR module uses the great bulk of the adder's power. Consequently, this module was designed to minimize power consumption while avoiding voltage drop. As illustrated in Fig. 1(b), the power consumption of the enhanced XNOR circuit is significantly reduced by building a weak inverter (with transistors having narrow channels).

Level restoring transistors Mp3 and Mn3 are utilized, allowing the output signals' levels to fluctuate freely [Fig. 1(b)]. A large number of XOR/XNOR architectures have already been reported ([7], [12–14]). The XOR/XNOR outlined in [12–14] uses four transistors, albeit at the cost of a slight logic swing. But unlike the 4 T XOR/XNOR that was disclosed in [12–14], the 6 More transistors are needed for the T XOR/XNOR in [7] in order to produce a greater logic swing. The XNOR module in this study uses 6 T, just like the 6 T XOR/XNOR [7], but the transistor arrangement is different. This study introduces a modified XNOR that is high-speed (with acceptable logic swing) and low-power compared to a 6 T XOR/XNOR [7].

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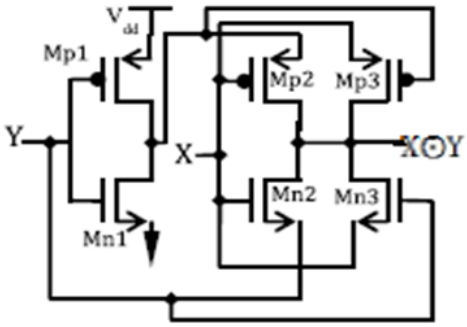


Fig. 4.2. Modified xnor module: a block diagram

4.2. CARRY GENERATION MODULE

Transistors Mp7, Mp8, Mn7, and Mn8 are used in the suggested circuit to carry out the output carry signal, as shown in Fig. 1(c). Between the input carry signal (Cin) and its destination, there is just one transmission gate (Mn7 and Mp7). By using robust transmission gates, carry signal propagation delays were further decreased (the channel width of transistors Mn7, Mp7, Mn8, and Mn8 was made big)..

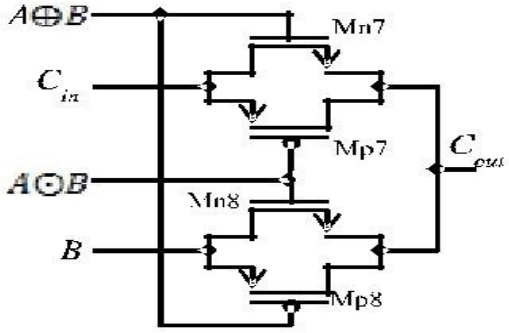


Fig.4.3. Carry generation module schematic

4.3. OPERATION OF THE PROPOSED FULL ADDER WITH SIMULATION TEST BENCH SETUP

Fig. 2 shows the detailed diagram of the entire adder. XNOR modules are utilized to implement the sum output of the entire adder. The controlled inverter composed of Mp2 and Mn2 transistors may be effectively developed by utilizing the output B' from the inverter composed of Mp1 and Mn1 transistors. The output of this regulated inverter is equal to the XNOR of A and B. The voltage drop they were producing was fixed by employing two pass transistors, Mp3 and Mn3. Using pMOS transistors (Mp4, Mp5, and Mp6) and nMOS transistors (Mn4, Mn5, and Mn6), the second stage of an XNOR module is realized to implement the entire SUM function. Cout generation's prerequisites have been determined by examining the truth table of a fulladder as follows:

If, A = B, then Cout = B; else Cout = Cin

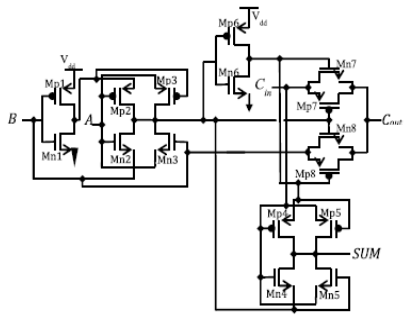


Fig.4.4. Extensive Adder Circuit Diagram

The A and B parity of the inputs is checked by a B function. If and only if a transmission gate is realized using transistors Mp8 and Mn8, then Cout is equal to B. Otherwise, the input carry signal (Cin) is reflected as Cout by a second transmission gate composed of transistors Mp7 and Mn7..

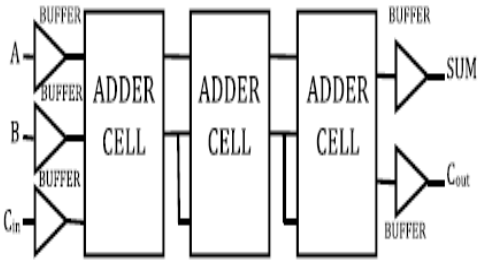


Fig4.5. Establishment of a Mock-Up Test Bench

When a single-bit adder cell is used in real-time, its optimal performance might be compromised. This is due to the possibility of an erroneous input signal level from the driver adder cells to the driven cells in a cascaded system. The circuit may fail as a result of the cumulative signal degradation at low supply voltages.Figure 3 shows the configuration of a realistic simulation environment used to assess the suggested full adder's performance in VLSI applications. To provide a more realistic environment, buffers are introduced to the input and output of the test bench [18, 25]. In order to eliminate the impact of input capacitance and preserve a steady loading condition, buffers are applied to an adder cell's inputs and outputs. Numerous.

4.4. PERFORMANCE ANALYSIS OF THE PROPOSED FULL ADDER

With an emphasis on the hybrid design approach [1], [2], and [19], simulations of both 90-nm and 180-nm technologies were conducted on the proposed full, and the outcomes were contrasted with those from other potential adder designs documented in [1]–[11] and [15–24]..

TRANSISTOR SIZES OF PROPOSED FULL ADDER

Transistor Name	180nm technology		90nm technology	
	Width (W) (nm)	Length (L) (nm)	Width (W) (nm)	Length (L) (nm)
Mn1, Mn6	400	180	120	90
Mp1, Mp6	800	180	240	90
Mn2, Mn3	400	180	120	90
Mp2, Mp3	800	180	360	90
Mn4, Mn5	400	180	120	90
Mp4, Mp5	400	180	120	90
Mn7, Mn8	400	180	360	90
Mp7, Mp8	400	180	600	90

In order to maximize power and delay in the circuit, the power-delay product (PDP), or energy consumption, has been minimized in the example shown. Transistors in the transmission gates between Cin and Cout were found to be mostly responsible for the design's carry propagation latency improvement, but the transistors in the inverter circuits were found to be primarily responsible for the design's power consumption. The transistor sizes for the suggested full adder circuit in both the 90 nm and 180 nm technologies are shown in Table I..

4.5. SCHEMATIC DIAGRAM OF THE PROPOSED FULL ADDER

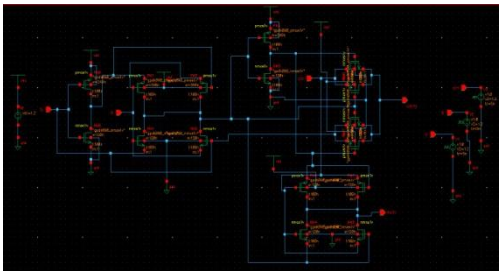


Fig.4.6. A Draught Circuit Diagram for a Full Adder

4.6. Timing diagram

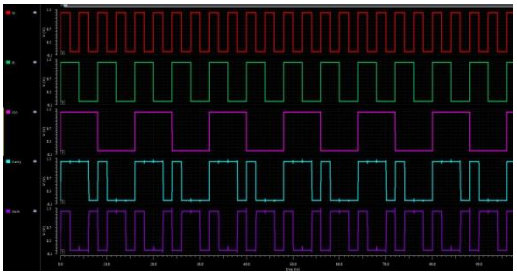


Fig.4.7. Schematic of the Proposed Full Adder's Timing

V. RESULTS AND DISCUSSIONS

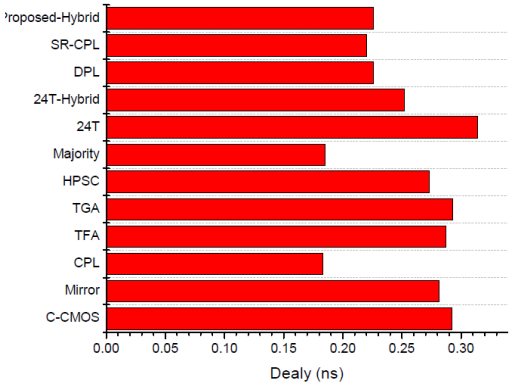


Fig. 5.1 THE 180-NITUDE TECHNOLOGY DELAY

In the graph above, we can observe that the suggested hybrid system has a delay of 0.226 ns in comparison to other systems constructed using 180 nm technology..

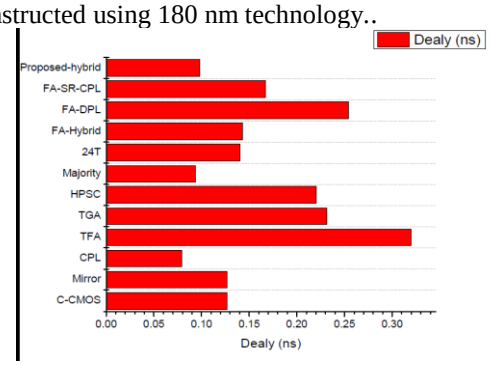


Fig. 5.2 SLOW PROGRESS ON 90 NM TECHNOLOGY

As can be observed from the graph above, the proposed hybrid system has a latency of 0.10 ns, which is substantially less than other systems constructed using 90 nm technology..

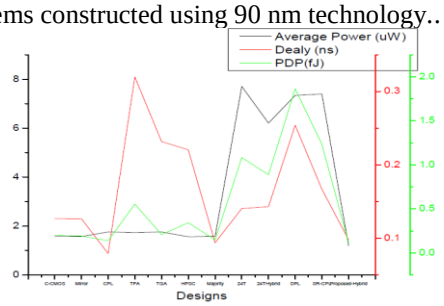


Fig. 5.3 90nm Technology Power Delay and PDP Averages

In terms of average power, latency, and PDP, the suggested hybrid system is contrasted with current systems constructed using 90nm technology in the graph above. The proposed hybrid system has a power consumption of 1.1965 uW, a latency of 0.098 ns, and a power delay product (PDP) of 0.117 f J. When compared to other existing systems, it is observed to function effectively..

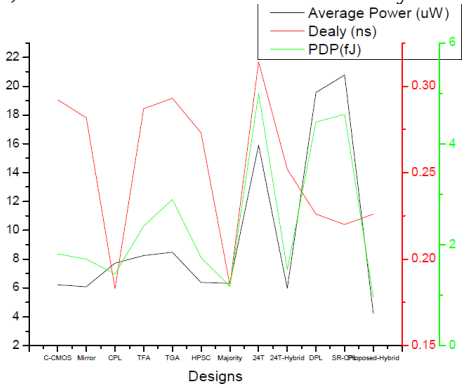
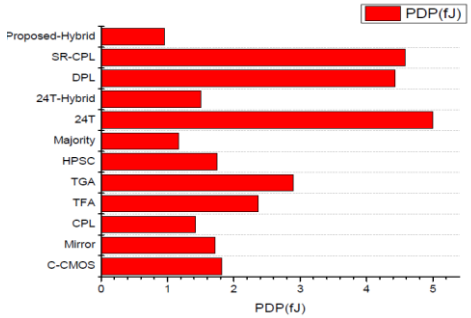


Fig. 5.4 180nm Technology Power Delay and PDP Averages

The preceding graph compares the proposed hybrid system to existing systems built with 180nm technology in terms of average power, latency, and PDP. The PDP (power delay product) for the proposed hybrid system is 0.956 f J, the delay ns is 0.226 ns, and power consumption is 4.232 uW. When compared to other existing systems, it is observed to function effectively..

PDP IN 180NM TECHNOLOGY



Using 180nm Technology PDP in Figure 5.5 The PDP of the suggested hybrid system is contrasted with that of current systems constructed using 180nm technology in the accompanying diagram. The suggested hybrid system has a very low PDP (0.956fJ) in comparison to similar systems.

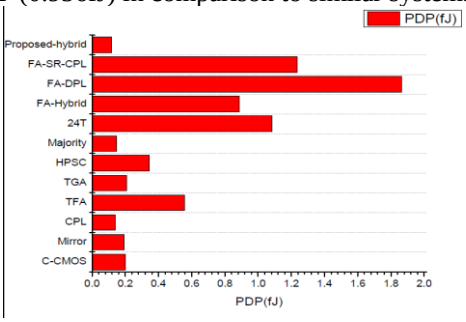


Fig. 5.6 Technology for PDP at 90 nm

The PDP for the suggested hybrid system and current systems constructed using 90nm technology are shown above for comparison. The proposed hybrid system has a very low PDP (0.117fJ) in comparison to similar systems.

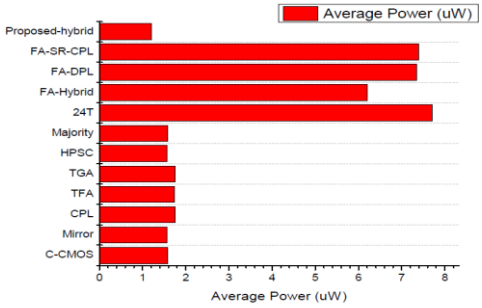


Fig. 5.7 Standard Power Consumption at 90 nm

The power consumption of the suggested hybrid system and competing systems based on 90nm technology is depicted above. When compared to other systems, the suggested hybrid system's power consumption is significantly lower (1.1965uW).

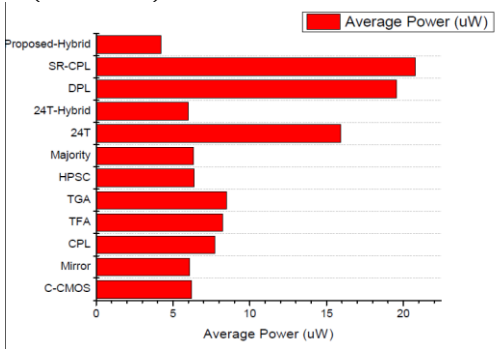


Fig. 5.8 Standard Power Consumption at 90 nm

Above, you can see a comparison between the energy consumption of the proposed hybrid system and that of other systems built with 180nm technology. When compared to previous systems, the power consumption of the proposed hybrid system is quite low, at only 4.232uW.

VI. CONCLUSION

- The design of a hybrid 1 bit full adder that blends transmission gate logic and CMOS is presented in this study. In this instance, a weak CMOS inverter is used by the XNOR module to save power usage.
- By using strong transmission gates in the carry generating module, signal propagation delays can be reduced..

FUTURE SCOPE

By carefully placing buffers throughout the addition operation, the suggested complete adder can also be utilized to produce a 32-bit carry propagation adder.

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