DESIGN AND PERFORMANCE ANALYSIS OF SINGLE ELECTRON TRANSISTOR MODELS

B. Abraham David
PG Scholar, Department of ECE, Holy Mary Institute of Technology & Sciences, Medchal, TS, India

Y.David Solomon Raju
Associate Professor, Department of ECE, Holy Mary Institute of Technology & Sciences, Medchal, TS, India

Abstract:

Circuits with SETs are also able to achieve a lot of new functionalities with less number of devices through novel design methodologies. However, pure SET based circuits have very limited applications due to SET's low current drivability, high output impedance, high sensitivity to background charges, small voltage gain and extremely low temperature operation, so that direct application to practical circuits is impossible, to overcome this problem and to investigate the robustness and fastness of the novel design. In this paper, a customized design is performed for a room temperature operable circuit in hybrid SET CMOS logic with considerably low power consumption. A new basic CMOS-SET logic gates which are capable for designing Half Subtractor and Full Subtractor, temperature is designed using T-SPICE simulation software.

Keywords*: Half Subtractor, Full Subtractor, Single Electron transistor, T-Spice*

1.Introduction

The continuous scaling of MOSFET device dimensions is the primary catalyst for this stunning growth of modern semiconductor industry. As the scaling increases, packing density increases, production cost decreases, circuit switching speed increases and power consumption decreases, the size of the transistor, the basic building blocks in integrated circuits (ICs) decreases with each new operation of technology. As the transistor size is scaled down, the chip area required for a given circuit is reduced, so that more chips can be manufactured on a single silicon wafer substrate, resulting in lower manufacturing cost per chip. Circuit operation speed also improves, because of reduced capacitance and higher transistor current density. As long as downward scaling of MOS devices remains strong, it would face restrictions due to increased sub-threshold leakage current, increased gate oxide leakage, increased transistor parameter variability and reliability.

In cryptography, encrypt messages with help of factoring large numbers; the time of factoring problem is arising in classical design flow. Therefore, quantum computing made the feasibility on factoring problem. Here we will address the issues in quantum computing, that of qualitative differences between quantum and the classical models for computation and a quantum model for computation. Shor's quantum algorithm achieved factoring numbers through quantum computation and the researcher's works on arbitrary unitary operations to down into simpler ones. A quantum logic gates operate on q-bits, which are able to simulate arbitrary, unitary operations like classical logic. A property of unitary matrices having a product of unitary logic gate and two of them remains unitary. We introduce the universal quantum logic gates, the XOR, the NOT gates.

This paper is organized as follows, section 1 presents the need and scope of the work, section 2 presents the basic literature survey for the current work, section 3

presents the schematic deign of proposed SET model with results discussed in section 4.

2.Related Work

The first observation of a Coulomb staircase at room temperature is proposed by Schonenberger et al [1]. Even in the early stages of single-electron research, a huge functions of single-electron devices, from quantum metrology, to sensitive electrometers, to transistors, memory and logic devices for integrated circuit applications, were acknowledged by Likharev [2]. The effect single-electron tunneling in semiconductor devices was first observed in the conductance of a one-dimensional (1-D) channel of silicon MOSFET at low temperature, by Scott-Thomas et al., [3], and the follow up by Van Houten and Beenaker [4].

For a long time, semiconductor hetero structures have been used to realize two dimensional electron gases (2DEGs) in HEMTs (high-electron mobility transistor). Hetero-structure single-electron transistors are closely related to HEMTs, with the minor difference that the 2DEG is patterned by electrostatic contacts (Schottky contacts) at the top of the device to create a small charged island. Small islands were also defined by lithography in the two-dimensional electron gas (2DEG) layer in III-V hetero structures.

At low temperatures, quantum confinement effects take place in the island and form a quantum dot, which is separated from the source and drain regions by tunnel barriers. In these devices, patterned surface gates were used to create the tunnel barriers, by depleting sections of the 2- DEG in AlGaAs/GaAs hetero structure material Meirav et al., [5], Kouwenhoven et al [4]. This led to the term artificial atoms for this kind of structure. GaAs/AlGaAs single electron transistor (SET) prototypes were reported in 1987. These devices had islands several hundreds of nanometers across because of technological limitations.

In 2010, El-Sayed A.M. Hasaneen [6] presents a new exact analytical model for single electron transistor (SET) applicable for circuit simulation. It has been developed based on orthodox theory of single electronics using master equation where a scheme has been suggested to determine the most probable occupied electron states. This model is more flexible and is valid for single or multi-gate, symmetric or asymmetric devices and can also consider the background charge effect.

In 2013, Anindya Jana [7] proposed a methodology to build hybrid circuits consisting of single electron transistors (SETs) and CMOS interfaces. In this work a room temperature operable Hybrid CMOS–SET inverter, NOR, NAND, XOR gate and their Voltage Transfer Characteristics (VTCs) are presented. In 2015 Basanth Singh. N [8]., proposed a methodology to build a hybrid circuits of adders, multiplexers, registers using SET-CMOS concepts.

3.Proposed Methodology

The most exceptional property of Single electron transistor is to switch the device from the insulating state to the conducting state by accumulation of one electron to the gate electrode. On the contrary conventional MOSFET desires about 2000-20,000 electrons for proper operation. Therefore, single-electron devices have faster switching time than

conventional MOSFETs. Moreover, it consumes ultra-low power (four five decades lower than CMOS) for its operation due to its ultra-small size.

In spite of SETs unparalleled advantages, the limitations of low current drivability, small gain, lack of room temperature operable technology and background charge effect became challenges in future silicon technologies. Here need the advantages of CMOS technologies such as high gain, high driving speeds to compensate the intrinsic drawbacks of SET. It can be manifested from the literature review that many analyses have been done at the hybrid SET-CMOS circuit.

SET is operated very small drain voltages ($V_{ds} < \frac{e}{c_\varepsilon}$) than MOSFET devices, so drain current of SET is in Nano-ampere range. Therefore, some design rules have to be obeyed for practical hybrid CMOS-SET co-design. There is a relationship between the bias current and the output voltage (VDS) of a constant current biased SET. As the bias current increases, VDS increases, the dynamic range of the VDS variation decreases, and influence of the temperature on the output voltage decreases. That's why SET and CMOS is designed in following way to optimize Hybrid CMOS-SET.

Figure 1 is the schematic of the hybrid SET CMOS inverter, where a SET only drives CMOS inverter with interconnect parasitic and table 3.2 shows the parameter used for device simulation at room temperature. It is formed by replacing NMOS transistor by SET and PMOS acting as the load resistance of a SET.

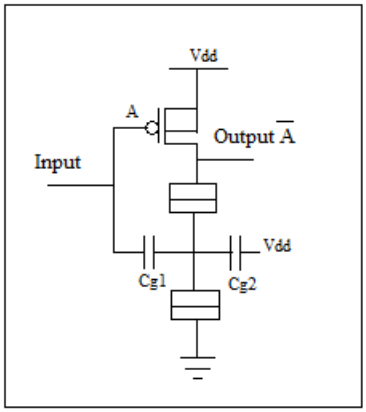

Figure 1: Hybrid SET-CMOS inverter circuit diagram

The circuit consists of 9 hybrid SET-CMOS transistors and the supply voltage VDD is considered as 800mv and Vi are 0V ("low") or 1V ("high"). The input voltages V (A, B) are applied through SET-CMOS counterparts of through gates, the output signal of the half subtractor are taken from the source and drain of SET-CMOS gates, as difference and borrow.

Table 1: Parameter used in Simulation process

Device	Parameter
SET	CG1=0.025aF CG2=0.127aF CTD=C_{Ts}=0.15aF R_{TD}=R_{TS}=1MΩ

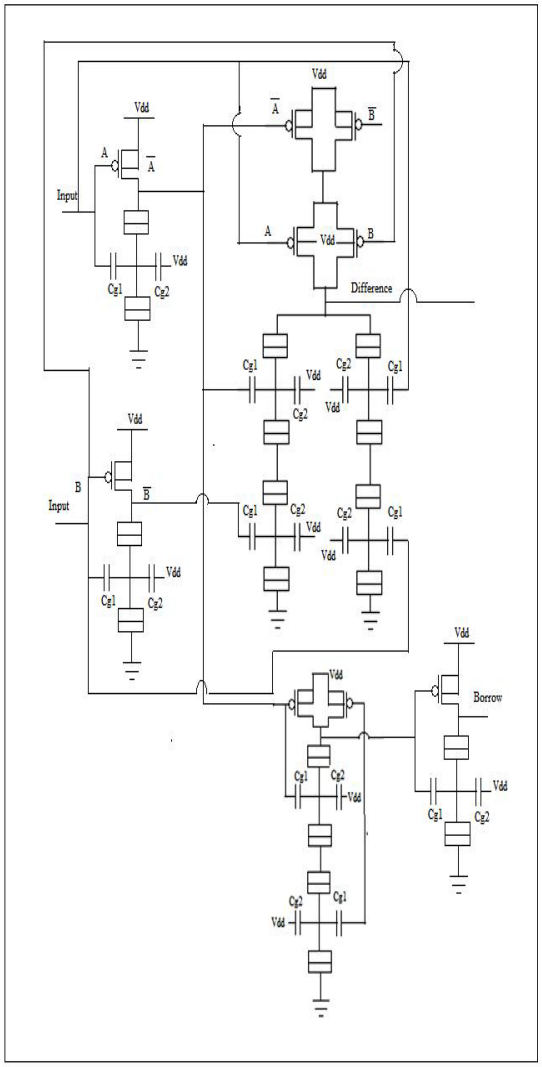

Figure 2: Hybrid CMOS-SET Half Subtractor circuit

We have verified the proposed half subtractor implementation by simulation. For half subtractor we used the following circuit parameters Cg1 = 0.2aF, Cg2= 0.12aF, $C_{TD} = C_{TS}$ = 0.15aF and $R_{TS} = R_{TD}$ = 1MΩ. The simulation results are depicted in figure 4.3 and only one output of the circuit is depicted for reference

4. Experimental Results

To evaluate the performance of the designed circuits all the designs of circuits are synthesized and verified using Xilinx 10.1SE software tool

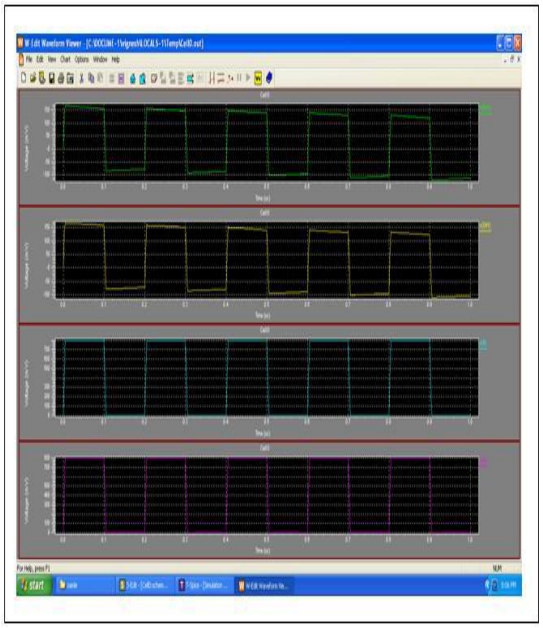

Figure 3: Simulation result of hybrid Half Subtractor

Delay Product Analysis A noticeable reduction in power consumption is presented in comparison with so called CMOS logic over following Table 2

Table 2: Comparison of average power consumption (Watt-sec) of half subtractor

S.NO	Supply Voltage	CMOS Model	Hybrid CMOS-SET
1	0.6	2.661e-09	5.43e-10
2	0.8	3.771e-9	6.05e-10
3	1.0	4.675e-9	7.765e-10
4	1.2	1.035e-8	3.109e-9

5	1.4	1.431e-8	3.707e-9

At minimum supply voltage, power consumption of CMOS model and SET-CMOS model is 2.6661E-009 watt and 5.343E-010 watt and at maximum supply voltage, power consumption is 1.4317E-008 watt and 3.707E-009 watt. It says that power consumption is increased by increasing supply voltage, which is a satisfactory factor since power consumption is directly proportional to supply voltage, and is reduced by decreasing supply voltage. When comparing the power consumption from CMOS model and SET-CMOS model of half subtractor, the proposed design shows low in terms of power consumption. Since power and high speed operation are inversely proportional to Rt, its value needs to be optimized for best performance. Power delay product for conventional CMOS based circuit and SETCMOS based hybrid counterpart is tabled below in table 3

Table 3: Power delay (Watt-sec) product of half subtractor

S.NO	Supply Voltage	CMOS Model	Hybrid CMOS-SET
1	0.6	1.89e-12	3.63e-13
2	0.8	3.765e-12	4.998e-13
3	1.0	5.678e-12	7.233e-13
4	1.2	8.967e-12	10.215e-13
5	1.4	10.24e-12	12.58e-13

At minimum supply voltage, power delay of CMOS model and SET CMOS model is 1.89E-012 watt-sec and 3.3638E-013 watt-sec. and at maximum supply voltage, power delay is 10.243E-12 watt-sec and 12.589E-013 watt-sec. It says that power delay is increased by increasing supply voltage, which is a satisfactory factor since power delay is directly proportional to supply voltage, and is increased by increasing supply voltage. When comparing the power delay from CMOS model and SET-CMOS model of half subtractor, the proposed design shows low in terms of power delay.

Table 4: Voltage Versus time delay (sec) of half subtractor

S.NO	Supply Voltage	CMOS Model	Hybrid CMOS-SET
1	0.6	2.98e-08	1.894e-09
2	0.8	2.995e-08	1.569e-09
3	1.0	2.003e-08	1.432e-09
4	1.2	2.002e-08	1.231e-09
5	1.4	1.997e-08	1.002-09

At minimum supply voltage, delay time of CMOS model and SET-CMOS model is 2.985E-008 sec and 1.894E-009 sec and at maximum supply voltage, delay time is 1.998E-008 sec and 1.002E-009sec. It

explains that the delay time is decreased by increasing supply voltage, which is a satisfactory factor since delay time is inversely proportional to supply voltage, and is reduced by increasing supply voltage. When comparing the delay time from CMOS model and SET-CMOS model of half subtractor, the proposed design shows low in terms of delay time.

5. Conclusions

In the near future, the eventual end to the roadmap of semiconductors is anticipated which hinders further scaling of CMOS technology. Alternative approaches are desired to satisfy those expectations to increase in the digital applications. This work is devoted in pursing solutions to the simulation issue of single electronics that come up as Single Electron Devices (SEDs) and are increasing by involved in next generation circuit architecture design. It has been proved that the SEDs models are more appropriate for time complexity and accuracy. The work also explored the characteristics of SE-based circuits and proposed a hybrid model that could be used to estimate and analyze its output both efficiently and accurately.

References

[1] Schonenberger C., van Houten H. and Donkersloot H.C.," Single electron unneling observed at room temperature by scanning-tunneling microscopy", Euro phys Letter 20: 249–254, 1992.

[2] Likharev K.K., "Correlated discrete transfer of single electrons in ultra-small tunnel junctions," IBM J Res Develop 32: 144–158, 1998.

[3] Scott-Thomas J.H.F., Kastner M.A., Antoniadis D.A., Smith H.I. and Field S., "Si metal- oxide semiconductor field effect transistor with 70- nm slotted gates for study of quasi- one-dimensional quantum transport", Journal Science Technology B 6: 1841–1844, 1998.

[4] Van Wees B.J., Van Houten H., Beenakker C.W.J., Williamson J.G., Kouwenhoven. L.P., Vander Marel D. and Foxon C.T., "Quantized conductance of point contacts in a two-dimensional electron gas", Phys Rev Letter 60: 848–850, 2004.

[5] Meirav U., Kastner M.A. and Wind S.J., "Single-electron charging and periodic conductance resonances in GaAs nanostructures", Physics Rev Letter 65: pp.771–774, 1990.

[6] El-Sayed, A.M. Hasaneen, Mohamed A.A. Wahab, and Mohamed G. Ahmed,"Exact analytical model of single electron transistor for practical IC design Microelectronics Reliability 51, pp.733–745, 2011

[7] Anindya Jana,N.,Basanta Sing, Jamuna K. Singh and Subir Kumar Sarkar , "Design and simulation of hybrid CMOS SET circuits", Microelectronics Reliability, Elsevier, Issue 4, Vol. 53, pp. 592-599, 2013

[8] Amit Jain, Arpita Ghosh, Basant Singh, N., and Subir Kumar Sarkar, "Stability and Reliability Analysis of Hybrid CMOS-SET Circuits –A New Approach", Journal of Computational and Theoretical Nanoscience, 2015.

[9] Dolan, G. J., and Fulton, T. A., "Observation of single-electron charging effects in small tunnel junctions", Phys. Rev. Letter, vol.59, pp. 109-112, 1987.

[10] Hiroshi Inokawa, and Yasuo Takahashi, "A Compact Analytical Model for Asymmetric Single-Electron Tunneling Transistors", IEEE Transactions on electron devices, vol. 50, no. 2, 2003

[11] Mahapatra. S., Vaish. V., Wasshuber. C., Banerjee. K., and Mihai Ionescu. A., "Analytical modeling of single electron transistor for hybrid CMOS-SET analog IC design," IEEE Transactions on Electron Devices, vol. 51, pp. 1772- 1782, 2004.

[26] El-Sayed, A.M. Hasaneen, Mohamed A.A. Wahab, and Mohamed G. Ahmed,"Exact analytical model of single electron transistor for practical IC design Microelectronics Reliability 51, pp.733–745, 2011.

[13] Meindl, J.D., Q, Chen and Davis. J.A., "Limits on Silicon Nano electronics for Tera-scale integration," Science, Vol.293, Pg.2044-2049, 2001.

[14] Amarnath Reddy, and Manoj, K.V., "Design of logic circuits using Reversible gates", IJETT, volume 16, pp. 394-396, 2014.