AN IMPROVED POWER SUPPRESSION APPROACH FOR MULTIPLIER USING XILINX TOOLS

S.*Pavan Kumar*
PG, Scholar,
Department of ECE,
Holy Mary Institute of Technology & Sciences, Medchal, TS, India

Y.B.T.Sundari
Assistant Professor, Department of ECE, Holy Mary Institute of Technology & Sciences, Medchal, TS, India

Dr.K.Kanthi Kumar
Associate Professor, Department of ECE, Holy Mary Institute of Technology & Sciences, Medchal, TS, India

Abstract: - *This paper provides the experience of applying an advanced version of our former spurious power suppression technique (SPST) on multipliers for high-speed and low-power purposes. To filter out the useless switching power, there are two approaches, i.e., using registers and using AND gates, to assert the data signals of multipliers after the data transition. The SPST has been applied on both the modified Booth decoder and the compression tree of multipliers to enlarge the power reduction. The simulation results show that the SPST implementation with AND gates owns an extremely high flexibility on adjusting the data asserting time which not only facilitates the robustness of SPST but also leads to a 40% speed improvement. Adopting a 0.18- m CMOS technology, the proposed SPST-equipped multiplier dissipates only 0.0121 mW per MHz in H.264 texture coding applications, and obtains a 40% power reduction.*

Key words: *H.264, low-power, multiplier, spurious power suppression Technique (SPST).*

I. INTRODUCTION

Lowering down the power consumption and enhancing the processing performance of the circuit designs are undoubtedly the two important design challenges of wireless multimedia and digital signal processor (DSP) applications, in which multiplications are frequently used for key computations, such as fast Fourier transform (FFT), discrete cosine transform (DCT), quantization, and filtering. To save significant power consumption of a VLSI design, it is a good direction to reduce its dynamic power that is the major part of total power dissipation.

The designs [1]–[7] are existing works that reduce the dynamic power consumption by minimizing the switched capacitance. The design [1] proposes a concept called partially guarded computation (PGC), which divides the arithmetic units, e.g., adders, and multipliers, into two parts, and turns off the unused part to minimize the power consumption. The reported results show that the PGC can reduce power consumption by 10% to 44% in an array multiplier with 30% to 36% area overheads in speech related applications. Design [2] proposes a 32-bit 2’s complement adder equipping a master-stage flip-flop and a slave-stage flip-flop for both operands of the adder, a dynamic-range determination (DRD) unit, and a sign-extension unit. This design tends to reduce the power dissipation of conventional adders for multimedia applications. Additionally, design [3] presents a multiplier using the DRD unit to select the input operand with a smaller effective dynamic range to yield the Booth co-codes. The direct report of [3] shows that the multiplier cacan save over 30% power dissipation than conventional ones. Design [4] incorporates a technique for glitching power minimization by replacing some existing gates with functionally equivalent ones that can be “frozen” by asserting a control signal. This technique can be applied to replace layout-level descriptions and guarantees predictable results. However, it can only achieve savings of 6.3% in total power dissipation since it operates in the layout-level environment which is tightly restricted. The design [5] proposes a double-switch circuit-block switch scheme capable of reducing power dissipation during down time by shortening the settling time after reactivation. The drawbacks of the scheme are the necessity for two independent virtual power rails and the necessity for two additional transistors for switching each cell. Design [6] and design [7], respectively, study signal gating schemes for adders and multipliers. Design [6] presents the arithmetic details about the signal gating schemes and illustrates 10% to 45% power reduction for adders.

Furthermore, this study examined some modern multiplier or MAC designs [8]–[15]. The design [8] includes three techniques, i.e., the signal flow optimization (SFO), left-to-right leapfrog (LRLF) structure, and upper/lower split structure, to optimize the array multipliers. The SFO and LRLF techniques are used for signal balancing of the partial product reducing (PPR) stage in a multiplier. Moreover, the upper/lower split structure is used to shorten the path of the PPR stage to prevent the snowballing glitch effect. Thus, design [8] can save about 20% power dissipation when compared with conventional right-to-left multipliers. Design [9] turns off some columns in the multiplier array whenever their outputs are known, thus saving 10% power consumption at the cost of 20% area overhead for random input under a 0.35-_m CMOS technology. Design [10] uses a DRD unit to detect the dynamic range of the inputs, and adopts three separate Wallace trees for the 4x4, 8x8, and 16x16 multiplications which certainly induce area and capacitance penalties. Under a 0.13-_m CMOS technology, design [10] can obtain a 20% power reduction over the conventional multiplier at a cost of 44% in area overheads. Design [11] proposes a 32-bit SIMD MAC unit which is a co processor to the Intel X-Scale microprocessor. Under a 0.18-_m CMOS technology, [11] presents that the processor dissipates 450mWat 600 MHz with 1.3-V supply voltage. Design [12] is a vector MAC unit that can perform one 64x64, two 32x32, four 16x16, or eight 8_8 signed/unsigned multiply-accumulations. Design [13] involves a fixed-width 32-bit left-to-right multiplier which obtains an 8% speed improvement, a 14% power reduction, and a 13% area saving. Meanwhile, design [14] explores a design methodology for high-speed modified Booth multipliers. Finally, design [15] adopts an advanced 90-nm dual-Vt CMOS technology to implement a 16x16 bit multiplier that consumes 9 mW at 1 GHz with 1.3 V. Our former SPST is demonstrated to reduce 20% to 30% power dissipation of H.264 transform coding and some multimedia computations [16], [17]. The SPST uses a detection logic circuit to detect the effective data range of arithmetic units, e.g., adders or multipliers. When a portion of data does not affect the final computing results, the data controlling circuits of the SPST latch this portion to avoid useless data transitions occurring inside the arithmetic units. Besides, there is a data asserting control realized by using registers to further filter out the useless spurious signals of the arithmetic units every time when the latched portion is being turned on. Although this asserting control brings evident power reduction, it may induce additional delay which is the problem this study wants to solve. When implemented in a 0.18-_m CMOS technology, the proposed SPST-equipped multiplier dissipates only 0.0121 mW per MHz in H.264 texture coding applications, and obtains a 40% power reduction than the conventional multiplier. Compared with the former SPST, the new approach improves 40% speed of the SPST-equipped multipliers. The remainder of this

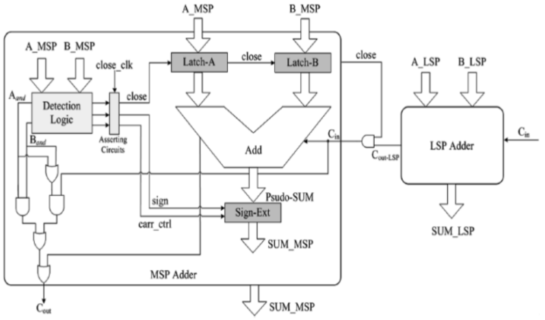


Figure 1: Low-power adder/subs tractor design example adopting the SPST.

paper is arranged as follows. Section II briefly reviews the former SPS technique, and then introduces the new implementing approach. Section III discusses the application of the SPST on multipliers. Section IV shortly describes the implementation and verification of this design, and then evaluates its performance. Finally, a conclusion is given in Section V.

II. PROPOSED SPURIOUS POWER SUPPRESSION TECHNIQUE (SPST)

The former SPST has been discussed in [16] and [17]. The main contribution of this paper is exploring two implementing approaches for the SPST and comparing their efficiency, which provide diverse reference materials for applying the SPST. For completeness of this paper and easy understanding for the readers, we simply review the former SPST first. In Fig. 1, the SPST is illustrated through a low-power adder/subtractor design example. The adder/subtractor is divided into two parts, i.e., the most significant part (MSP) and the least significant part (LSP). The MSP of the original adder/subtractor is modified to include detection logic circuits, data controlling circuits, denoted as latch-A and latch-B in Fig. 1, sign extension circuits, and some glue logics for calculating the carry in and carry out signals. The most important part of this study is the design of the control signal asserting circuits, denoted as asserting circuits in Fig. 1, following the detection logic circuits

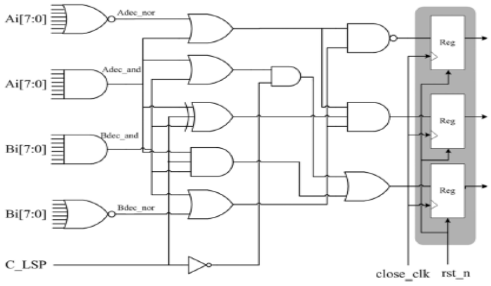
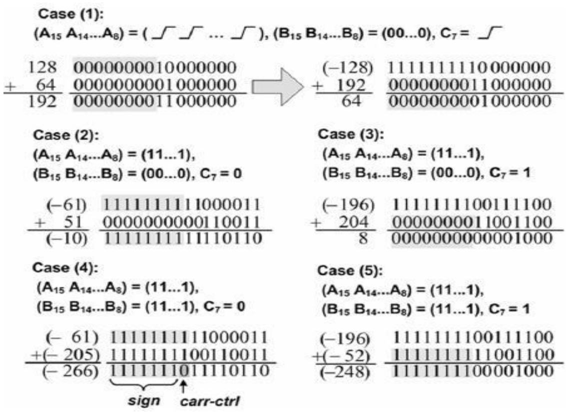


Figure 2: Detection logic circuits using registers to assert the control signals

Figure 2 the three output signals of the detection logic are given a certain amount of delay before they assert, demonstrated in the timing diagram shown in Fig. 3. The delay _, used to assert the three output signals, must be set in the range of < _ < _ to filter out the glitch signals as well as to keep the computation results correct, where and _, respectively, denote the data transient period and the earliest required time of all the inputs. The range of _ is also shown as the Using registers to control the signal assertions can obviously reduce the spurious power dissipation of adders/subtractors [16], [17].

However, the restriction that _ must be greater than to guarantee the registers from latching the wrong values of control signals usually decreases the overall speed of the applied designs. This issue should be noticed in high-end applications which demands both high-speed and low-power requirements.



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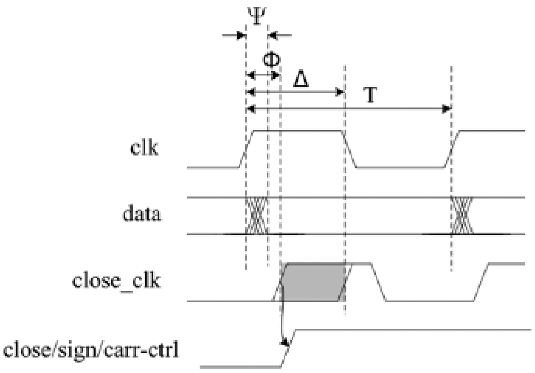

Figure 3: Timing diagram of the control signals of detection logic circuits after assertions.

To solve the previously mentioned problem, we adopt the other implementing approach of the control signal assertion circuits illustrated in the shadow area in Fig. 4, using an AND gate in place of the registers to control the signal assertion. The timing control of the delay in this implementation is slightly different from the one in the first implementation.

That is, the range of _ can be set as 0 < _ < _ to filter out the glitch signals and to keep the computation results correct, as well. This feature allows upper-level systems to assert the *close* signal with an arbitrarily short delay closing to the positive edge of the clock signal, which provides a more flexible controlling space for the delay. When speed is seriously concerned, this implementing approach enables an extremely high flexibility on adjusting the data asserting time of the SPST-equipped multipliers. Therefore, the proposed advanced shadow area in Fig. 3. Readers, who have interests in other details of this part, please refer to [16] and [17].

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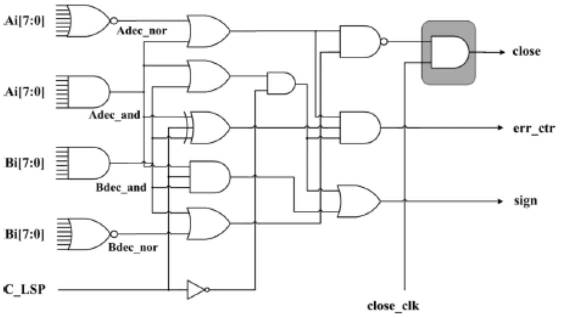


Figure 4: Detection logic circuits using an AND gate to assert the control signal.

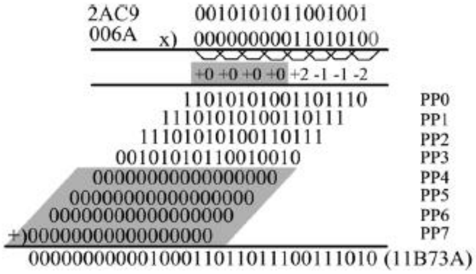


Figure 5: Illustration of multiplication using modified Booth encoding, where PP0 to PP7 denote the partial products.

III. LOW-POWER MULTIPLIER DESIGN

The proposed low-power multiplier is designed by equipping the SPST on a tree multiplier. There are two distinguishing design considerations in designing the proposed multiplier, as listed in the following.

Applying the SPST on the Modified Booth Encoder:

Figure 5 shows a computing example of Booth multiplying two numbers “2AC9” and “006A,” where the shadow denotes that the numbers in this part of Booth multiplication are all zero so that this part of the computations can be neglected. Saving those computations can significantly reduce the power consumption caused by the transient signals. According to the analysis of the multiplication shown in Figure 5, we propose the SPST-equipped modified-Booth encoder, which is controlled by a detection unit. The detection unit has one of the two operands as its input to decide whether the Booth encoder calculates redundant computations. As shown in Figure 6, the latches can, respectively, freeze the inputs of MUX-4 to MUX-7 or only those of MUX-6 to MUX-7 when the PP4 to PP7 or the PP6 to PP7 are zero, to reduce the transition power dissipation. Such cases occur frequently in e.g., FFT/IFFT, DCT/IDCT, and Q/IQ which are adopted in encoding or decoding multimedia data

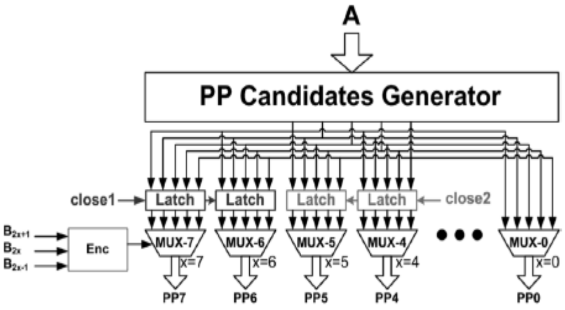


Figure 6: SPST-equipped modified-Booth encoder

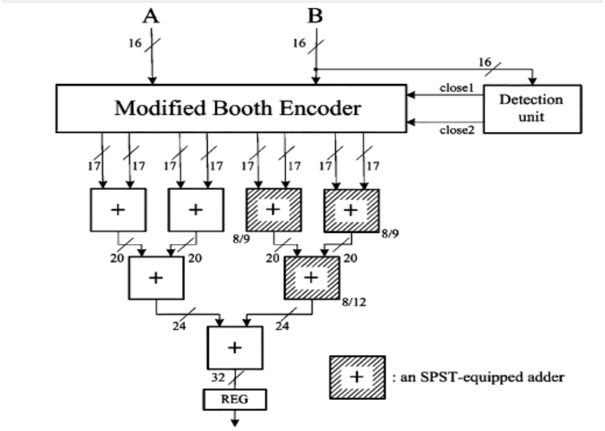
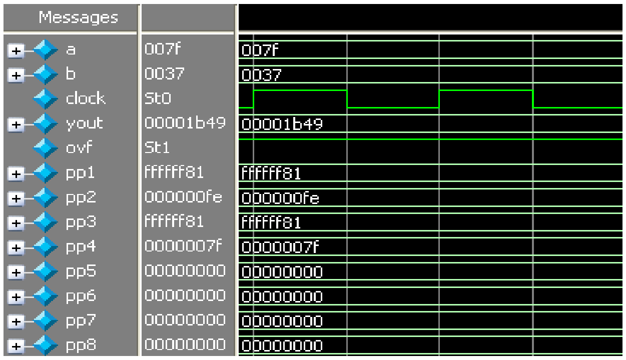


Figure 7: Proposed low-power SPST-equipped multiplier, where the fraction values denote the bit-widths of the MSP and LSP of the SPST-equipped adders.

Opportunities to reduce the spurious power dissipated in the compression tree. According to the redundancy analysis of the additions, we replace some of the adders in compression tree of the multiplier with the SPST-equipped adders, which are marked with oblique lines in Figure 7. The bit-widths of the MSP and LSP of each SPST-equipped adder are also indicated in fraction values nearing the corresponding adder in Figure 7.

IV. PERFORMANCE EVALUATION AND COMPARISON



```
Messages
a       007f      007f
b       0037      0037
clock   St0
yout    00001b49  00001b49
ovf     St1
pp1     ffffff81  ffffff81
pp2     000000fe  000000fe
pp3     ffffff81  ffffff81
pp4     0000007f  0000007f
pp5     00000000  00000000
pp6     00000000  00000000
pp7     00000000  00000000
pp8     00000000  00000000
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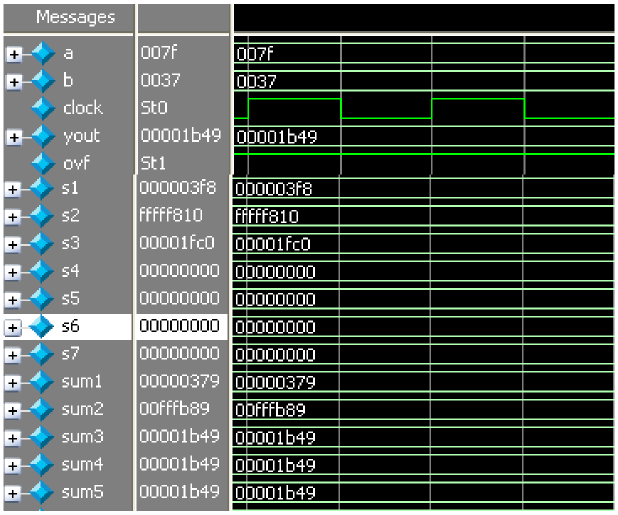
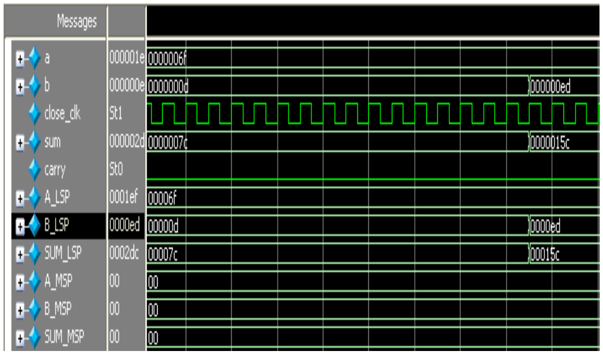
Figure 8: simulation result of booth encoder.



```
Messages
a        007f      007f
b        0037      0037
clock    St0
yout     00001b49  00001b49
ovf      St1
s1       000003f8  000003f8
s2       fffff810  fffff810
s3       00001fc0  00001fc0
s4       00000000  00000000
s5       00000000  00000000
s6       00000000  00000000
s7       00000000  00000000
sum1     00000379  00000379
sum2     00fffb89  00fffb89
sum3     00001b49  00001b49
sum4     00001b49  00001b49
sum5     00001b49  00001b49
```

Figure 9: Simulation result using SPST adder



```
Messages
a        000001e  0000006f
b        000000e  0000000d   000000ed
close_clk St1
sum      000002d  0000007c   0000015c
carry    St0
A_LSP    0001ef   00006f
B_LSP    0000ed   00000d     0000ed
SUM_LSP  0002dc   00007c     00015c
A_MSP    00       00
B_MSP    00       00
SUM_MSP  00       00
```

Figure 10: SPST adder technique

V. CONCLUSION

In this paper, we propose a multiplier adopting the new SSPST implementing approach, i.e., using AND gates in the detection logic unit. The simulation results show that the power reduction of the new approach, i.e., a 40% saving, is very close to that of the former approach Besides, the new approach leads to a 40% speed improvement when compared with the former one. When implemented in a 0.18-_m CMOS technology, the proposed SPST-equipped multiplier dissipates only 0.0121 mW per MHz in H.264 texture coding. In addition, this paper explores the performance of the proposed design under the conditions of different bit-width input data. The results also show that the new SPST approach not only owns equivalent low-power performance but also leads to a higher maximum speed when compared with the former SPST approach. Moreover, the proposed SPST-equipped multiplier also has better power efficiency when compared with the existing modern multipliers.

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